WHAT IS CLAIMED IS:

1. A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on those MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property, and the at least one predetermined property is such that at least one of the metal salicide regions formed in step (f) has at least one predetermined attribute.

2. The method of claim 1, wherein said at least one predetermined attribute of said at least one of the metal salicide regions is a sheet resistance.

3. The method of claim 1, wherein said at least one predetermined attribute of said at least one of the metal salicide regions is a conductivity.

4. The method of claim 1, where said at least one predetermined property of the metal layer is a thickness of said metal layer.

5. The method of claim 1, wherein the removal during step (d) of the metal layer from those MOS transistor structures where metal salicide exclusion

regions are to be formed, is performed in a manner significantly limiting metal salicide crawl over and under the metal salicide regions formed during step (f).

6. The method of claim 1, wherein the metal layer deposited in step (b) comprises metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum.

7. The method of claim 1 wherein the metal layer deposited in step (b) has a thickness in the range of 150 to 500 angstroms.

8. A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on those MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property, and the at least one predetermined property is such that at least one of the cobalt salicide regions formed in step (g) has at least one predetermined attribute.

9. The method of claim 8, wherein said at least one predetermined attribute of said at least one of the cobalt salicide regions is a sheet resistance.

10. The method of claim 8, wherein said at least one predetermined attribute of said at least one of the cobalt salicide regions is a conductivity.

11. The method of claim 8, where said at least one predetermined property of the cobalt layer is a thickness of said cobalt layer.

12. The method of claim 8, wherein the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, is performed in a manner significantly limiting cobalt salicide crawl over and under the cobalt salicide regions formed during step (g).